A Review of ARM Processor Architecture History, Progress and Applications

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Abstract: Globally, over 50 billion ARM architecture based embedded chips of 32-bit and 64-bit instruction set architecture are commonly used and produced in quantity perspective since 2014. In our daily life most of the people uses and depends upon a penalty of electrical and automotive devices which have now become an essential part of their daily life. Due to that reason embedded processors are used to build such devices which takes less silicone-space, provides efficient processing and less power.

Keywords— ARM history, RISC processor, modes of operation, ARM versions, CISC architecture, CPSR register, ARM Applications, ARM profile ARM architecture,, Cortex-R, Cortex M, Cortex-A, etc.

i. INTRODUCTION

Acorn RISC Machine, later Advanced RISC Machine is widely used reduced instruction set computer (RISC) family of computer processors, system on chip, system on module, smart phones, configured for various environment[1]. Acorn Computers firstly used the acronym ARM Acorn RISC Machine in 1983. In 1990 it was changed to "Advanced RISC Machines" due to incorporated of the company "Advanced RISC Machines Ltd." by the time of Initial Public Offering, Company name was modified to "ARM Holdings" surprisingly Apple was the joint venture partner at that time and has a long history with ARM[2]. Which is now owned by Japanese tele communions company "Softbank Group"[1]. Currently, ARM is world's top

Figure 1 ARM ECO SYSTEM

semiconductor IP Company who has shipped about 100 billion ARM based processors to date and has more than 1,100 partners. More than 95 % mobile devices are using the ARM powered processor[3].

As compared to CISC architecture which is more emphasis on hardware RISC architecture based processor has required fewer transistors and less silicon area. [12] In order to enhance the performance functions (floating point hardware, memory management functions, cache memory) of system a huge area of board is left free in RISC CPU Which brings improvement in cost, power consumption, and heat dissipation[4].

ii. FEATURES OF ARM ARCHITECTURE

When the primary ARM processor was introduced, only instances of reduced instruction set computing processor (RISC) were the Stanford MIPS and Berkeley reduced instruction set computing Processor. The ARM design has taken some of the features from Berkeley RISC design like a uniform register file load store architecture, 32-bit fixed-length instruction, and 3-address instruction formats[5].ARM architectural licensing provides the facility of designing their own processor cores with the help of instruction set of ARM. Such as Al- catel, Apple, Applied Micro, Atmel, Broadcom, Ca- vium, Nvidia, Nxp, Qualcomm Kyro, Raspberry Pi and Samsung electronics, X-Gene [6][7]

ARM architecture, blending of the simple hard- ware instruction sets that's stranded in RISC ideas but recalls some of key CISC features, such as improved code density, has made the ARM more power efficient and result in small silicone size (Furber) (Yokoyama, Schulze, Borges, & Mc Evoy, 2019). Embedded application gets the advantage of low cost and construction of simple pipeline.

iii. ARM ARCHITECTURE

Improvements in architecture of RISC allows Arm processors to achieve balance in less size of code, high performance, lowering the power consumption, and less region of silicon. Arm architecture has progressed with passing time, incorporating many levels of architecture in its history which are as follows [8].

- Security Extensions (Trust -Zone technology)
- Advanced-SIMD (NEON technology)[9]

- Virtualization-Extensions, introduced in Armv7A.[10]
- Crypto-Extensions, part of Armv8-A (ARM, developer.arm.com, n.d.).

ARM produces an entire family of CPUs that share shared (ISA) instruction sets architecture and programmer's models which have backward compatibility. CPUs applying the Arm Architecture follow to a particular series of the architecture[11]. Which are:

- ('A') profile or Architectural profile, is used for high performance industries such as mobile and enterprise.
- ('R') profile or Real-Time profile, used for embedded applications, healthcare, automotive and industrial control.
- ('M') Microcontroller profile or profile, used in the microcontroller, wearable, Internet of Things, single processing like controlling motor and power, sensor fusion [12].

The latest architecture Armv8 series architecture has three variations of the architecture relating processors aiming different markets:

- Latest generation of Arm architecture in A-profile is Armv8-A It indicate the overview of a 64-bit architecture beside the firm 32-bit architecture, and allows multiple stages of AArch32 and AArch64 support.
- Latest generation of Arm architecture in R-profile is Armv8-R .This architecture involved a Memory Protection Unit (MPU) and deterministic memory structure and supports the A32 and T32 instruction-sets architecture[13].
- Latest generation of Arm architecture in M-profile is Armv8-M.its mostly used in low cost embedded systems.it also support to other profiles by different exception handling technique and bring sup- ports to T32 instruction sets architecture[14].

Figure 2 ARM architecture evolution [3]

iv. ARM INSTRUCTION SET

ARM processors supports following 3 type of architecture instruction sets.

- A32 Instruction Set (A32-IS)
- T32 Instruction-Set (T32-IS)
- A64 Instruction-Set (A64-IS)

A32 Instruction-Set

A32 instructions or ARM instructions in preARMv8 architectures, are 32 bits wide, and are line up on

4-byte boundaries. A32 instructions only runs when previous instruction have set to special condition code such as N, Z, C and V flags[6]

Condition Meaning Code

N	Negative condition code. Set to 1 if result is negative
Z	Zero condition code. Set to 1 if the result of the instruction is 0,
C	Carry condition code. Set to 1 if the instruction results in a carry condition.
V	Overflow condition code. Set to 1 if the instruction results in an overflow condition.

Figure 3 A32 instructions Condition Code [8]

A64 Instruction Set (A64-IS)

The main support of A64-IS is the architecture of ARMv8-A and it Important feature are following:

- 5-bit clean decoder table based register specifiers.
- A32 and T32 Instruction
- 64-bit general purpose registers accessible at any time (total = 31).
- For improvement in performance and energy of general purpose registers modal banking is not implemented.
- Dedicated, zero-register available for utmost instructions [6]

v. ARM PROCESSOR MODES OF OPERATION

ARM used seven operating modes .Respectively has access to its individual stack space and a different subset of registers.

Mode	Description
Supervisor (SVC)	Entered on reset and when a Supervisor call instruction (SVC) is executed
FIQ	Entered when a high priority (fast) interrupt is raised
IRQ	Entered when a normal priority interrupt raised
Abort	Used to handle memory access violations
Undef	Used to handle undefined instructions
System	Privileged mode using the same registers as User mode
User	Mode under which most Applications/OS tasks run

Figure 4 ARM processor modes of operations [15]

vi. IMPORTANT REGISTERS

The internal hardware device of CPU is Register which not only stores binary data but also can be accessible rapidly than other locations in RAM. 13 general purpose registers are used in ARM like: One Stack Pointer (SP) and R0 to R12 registers. 1 Link Register (LR) R13. One Program Counter (PC), Return address of caller is hold by R14. One Current Program Status Register (CPSR) by register R15 [16], the ARMv6-M and ARMv7-M exception are, Banked SP and LR for two modes of supervisor registers. Two Banked SP and LR Abort Mode Registers. Two modes of undefined registers for the SP and LR banked. Two modes of interrupt

register for SP and LR banked. Seven register of FIQ mode for R8-R12 banked, LR and SP. Two registers of monitor mode for SP and LR banked. Six Saved Program Status Registers (SPSRs), 1 exception mode [16].

Figure 5 ARM processor important registers [19]

The 32-bit and 64-bit series of RISC ARM Processor cores is of ARM Cortex-A which are used for applications consisting of 32-bit ARM Cortex (A5, A7-A9, A12, A15, A17) and 64-bit ARM Cortex (A-53, A57, A72)[10] [18].

Application includes

- Server
- Automotive
- Embedded
- Smartphones
- Intelligent devices in your home
- Large-screen compute

vii. APPLICATION DOMAINS OF ARM PROCESSOR

Following are the application series of Cortex processor.

• ARM CORTEX-A SERIES PROCESSORS

Cortex-A series, deliver a range of solutions for devices responsible for the tasks of complex computing, like: rich Operating System (OS) hosting platform, and support of different software applications[17]

ARM Cortex-A75

Figure 6 6 ARM Cortex-A75 CoreSight p[5]

Table 1 ARMv8-A Architecture features comparison [1]

Core	Release	Revision	Decode	Pipeline depth	Out of order Execution	Branch Prediction	Execution port	L0 Cache	L1 Cache Inst + data (in KiB)	L2 Cache	L3 Cache
Cortex-A75	2017	ARMv8.2-A	3-wide	11-13	Yes 6-wide dispatch	Two-level	8?	No	64 + 64	256-512KiB/core	0-4 MiB
Cortex-A76	2018	ARMv8.2-A	4-wide	11-13	Yes 8-wide dispatch	Two-level	8	No	64 + 64	256+512KiB/core	1-4 MiB
Cortex-A77	2019	ARMv8.2-A	4-wide	11-13	Yes 10-wide dispatch	Two-level	12	1.5K entries	64 + 64	256+512 KiB/core	1-4 MiB

• ARM CORTEX-R SERIES PROCESSORS

Cortex-R series, deliver fast and deterministic processing and high performance, while meeting challenging real-time constraints in a range of situations. They combine those features in a performance, power and area optimization, making them the trusted choice in consistent systems demanding high error resistance[13]. Important series of cortex-R processors are Cortex-(R4,R5,R7,R8) and most advanced processor of this series is Cortex-R52 [7]Application includes:

- Automotive
- Robotics
- Industrial
- Transportation
- Healthcare

- Building automation

**ARM
Cortex-R52**

Figure 7 ARM Cortex-R52 CoreSight [3]

**ARM
Cortex®-M33**

Figure 8 CHIP BLOCK DIAGRAM of Cortex-M33[3]

Table 2 Cortex ARMv8-R Architecture features comparison[1]

ARM Family	ARM Architecture		ARM core	Release	Features	Cache (I/D), MMU	Typical MIPS @ MHz
Cortex-R	ARMv7-R	Cortex-R7	2013	Thumb/Thumb-2/DSP/optional VFPv3 FPU & Precision, 11-stage pipeline dual core running lockstep with fault logic/out of order execution/dynamic registered renaming/optional as 2 independent core, Real-time profile,	0-64KB/0-64KB. ? of 0-128KB TCM, opt. MPU with 16 regions.		2.50 DMIPS/MHz
Cortex-R	ARMv7-R	Cortex-R8	2016	Thumb-2, DSP, opt. floating-point with single & double precision, 11-stages pipeline with instruction per-fetch, MPU.	4-64KB, TCM (1MB), MPU with 24 regions.		2.50 DMIPS/MHz
Cortex-R	ARMv8-R	Cortex-R52	2018	Thumb-2, DSP, Floating-point with single & double precision and Neon, 8-stages pipeline with instruction per-fetch, Dual core lockstep, MPU.	4K-32K, 3 TCM (1MB), Level 1MPU (24 regions up & down 64-bytes), Level 2 MPU (24 regions with a little as 64-bytes).		2.16 DMIPS/MHz

Arm Cortex-M Series Processors

Improved for cost and power-sensitive microchip control unit (MCU) devices for applications of IoT, motor control, connectivity, smart metering, human interface devices, automotive and industrial control systems and medical instrumentation[19].

Important cortex-M series processor are:

SC300 Processor, SC000 Processor, Arm Design Start, Cortex-(M0,M3,M0+,M4,M7, and M23) and

the most latest and advanced processor of this series is Cortex-M33[12]. Application includes

- Processing of Audio
- Smart home/building/planet/enterprise
- Wearables and Sensor fusion
- control
- Internet of Things
- Single processing such as power and motor
- Connectivity

Table 3 Cortex ARMv8-M Architecture features comparison[3]

ARM Family	ARM Architecture	ARM core	Release	Feature	Cache(I/D),MMU	Typical MIPS @ MHz
Cortex-M	ARMv8-M	Cortex-M23	2016	Thumb-1 (most), Thumb-2 (sum), Trust zone, divide, Microcontroller profile	No TCM, 16 regions MPU (optional), Cache (Optional)	0.99 DMIPS/MHz
Cortex-M	ARMv8-M	Cortex-M33	2016	Thumb-1, Thumb-2, Saturated, Divide, FPU(SP), Co-processor, Microcontroller profile, DSP, TrustZone	No TCM, 16 regions MPU (optional), Cache (Optional)	1.50 DMIPS/MHz
Cortex-M	ARMv8-M	Cortex-M35P	2019	Thumb-1, Thumb-2, Saturated, DSP, FPU(SP), TrustZone, Microcontroller profile, Co-processor, Divide	Cache built in (optional 2-16KB),I-cache, no TCM, 16 regions MPU (optional)	1.50 DMIPS/MHz

viii. CONCLUSION

ARM architecture, blending of the simple hardware instruction sets that's stranded in RISC ideas but recalls some of key CISC features, such as improved code density, has made the ARM more power efficient and result in small silicone size. It is simple pipeline construction which is low cost and adds efficiency to modern VLSI technology and embedded applications and these technologies permits huge number of further components of system which can be incorporated on the same chip. The current low end ARM core is ARM9TDMI which is used excessively by a range of applications and also supports ARM 32-bit and Thumb instruction set of 16 bits which allows the user to tradeoff between density of high code and high performance. Most of the smartphones and electronics gadget which is the part of our daily life are now using this power. ARM processors towards ARM9 uses pipeline of 5 stages like: fetching,

decoding, execution, data memory access and register write.

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